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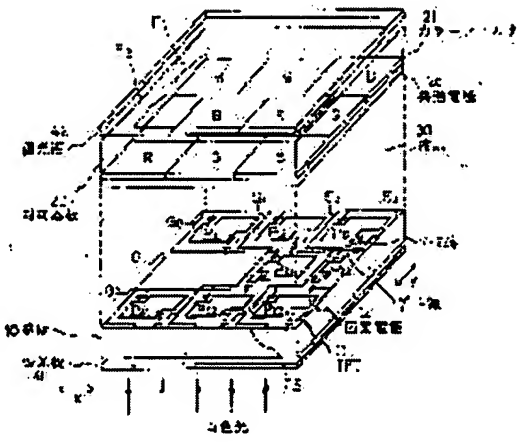
(54) ACTIVE MATRIX SUBSTRATE AND LIQUID CRYSTAL DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a high quality color liquid crystal display device in a delta array.

SOLUTION: A delta array is constituted by periodically arranging pixel regions (P11, P12 and P13) having pixel electrodes (12) corresponding to red, green and blue colors in an X direction while making the three colors as a unit and arranging the regions to be deviated for 1/2 period at odd and even number stages in a Y direction. When only the pixel electrodes of regions (P12, P22 and P32) corresponding to a same color are connected with respect to a same source line (S2), the regions are arranged in left and right alternatively with respect to the line. Among pixel regions arranged along the X direction, relative positions of a TFT (11), pixel electrodes, a first electrode section (C1) and a second electrode section (C2) of a holding capacitance (CS) are made the same. Among pixel regions arranged in the Y direction along source lines (S1, S2,



etc.), the relative locations of the TFT and the pixel electrode are inverted left and right every other stage. However, the relative position relationships of the holding capacitance and the first and the second electrode sections are made the same.

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* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the component structure of the active-matrix substrate used for a liquid crystal display, especially the structure of a retention volume capacitor. Moreover, it is related with the structure of the color liquid crystal display using the active-matrix substrate.
[Background of the Invention] The fundamental structure of the color liquid crystal display using a active-matrix substrate is shown in drawing 1 . the gate lines G0, G1, and G2 prolonged in the direction of X in the front face of a substrate 10 in drawing 1 -- with ... the source lines S1, S2, and S3 prolonged in the direction of Y -- these ... and source lines S1, S2, and S3 -- the ... and gate lines G1 and G2 and G3 -- the thin film transistor (it is hereafter called "TFT".) connected to two or more pixel electrodes 12 arranged in the location corresponding to an intersection with ..., and each pixel electrode 11 is formed.
[0002] and a selection period G1 and G2, i.e., gate lines, and G3 -- the liquid crystal part by volume CLC which consisted of liquid crystal 30 enclosed with the common electrode 26 formed in the opposite substrate 20 at the period whose TFT11 is an ON state, the pixel electrodes 12, and those gaps by the signal from ... the source lines S1, S2, and S3 -- the picture signal supplied from ... is written in. The picture signal written [the non-selection period, i.e., the period whose TFT11 is an OFF state,] in the liquid crystal part by volume CLC on the other hand at the selection period is held.
[0003] Here, in order to perform the high display of grace, it is called for that the maintenance property in a non-selection period is good. It is effective in it to form the retention volume capacitor CS in juxtaposition electrically to the liquid crystal part by volume CLC. About the retention volume capacitor CS, the configuration which forms the retention volume capacitor CS between the gate line of the preceding paragraph and the pixel electrode 12, or the configuration which forms the retention volume capacitor CS between the retention volume line (not shown to drawing 1) formed separately and the pixel electrode 12 is proposed.
[0004]
[Problem(s) to be Solved by the Invention] thus, the constituted retention volume capacitor CS, the pixel electrode 12, TFT11, and others accompany -- **** -- ** -- the pixel fields P11, P12, and P13 ... is constituted. In addition, although the pixel field is not formed between the pixel field P11 and the pixel field P31, there are also that by which the pixel field for blue is formed in the field, and a thing in which the dummy pixel field is formed here. The light filter 21 is formed in the opposite substrate 20. Generally a light filter 21 consists of the red filter R, a green filter G, and a blue filter B. These red filters R, the green filter G, and the blue filter B are repeatedly arranged in the display screen by making them into one unit. There is a stripe array, a mosaic array, or a delta array as array of a light filter 21. Here, the color array pattern of a delta array is shown in drawing 12 , and an example of the color array pattern of a mosaic array is shown to it at drawing 13 . In such a delta array and a mosaic array, since each color element distributes to homogeneity in the display screen, there is an advantage that a smooth image can be displayed, as compared with a stripe array.
[0005] As a liquid crystal display with which the delta array was used, there are some which were

indicated in the drawing 3 A of JP,3-64046,B, and there are some which were indicated in the drawings C-8 F of this official report as a liquid crystal display with which the mosaic array was used.
[0006] Three pixel fields P21, P22, and P23 corresponding to the red filter R, the green filter G, and the blue filter B make them one unit, and that for which the delta array was used among the liquid crystal displays indicated by this official report is periodically arranged in the direction of X, as shown in drawing 14 . However, the pixel fields P21, P22, and P23 in the pixel train of an even level eye shift only the distance which is equivalent to 1/2 period of said one unit to the pixel fields P11, P12, and P13 in a pixel train or the pixel fields P31, P32, and P33 of an odd level eye, and are arranged. For this reason, between the pixel train of an odd level eye, and the pixel train of an even level eye, they are the pixel fields P11, P12, and P13... Only the distance equivalent to a 1.5-pixel pitch has a center position in the condition of having shifted alternately with right and left.
[0007] Since any pixel field has the the same basic configuration, the pixel field P21 is explained to an example. In the pixel field P21, the source field 111 of TFT11 is connected to the source line S1, the gate electrode 113 is connected to the gate line G2, and the drain field 112 is connected to the pixel electrode 12.
[0008] Moreover, the 1st polar zone C1 electrically connected to the drain field 112 and the pixel electrode 12 of TFT11 and the 2nd polar zone C2 with the structure jutted out of the gate line G1 of the preceding paragraph in the direction of Y are formed in the pixel field P21. As for the ingredient of the 1st polar zone C1, the doped silicon silicon film is usually used. Through the dielectric film, the 1st polar zone C1 and the 2nd polar zone C2 counter, and are arranged as mentioned later. Thus, the retention volume capacitor CS is formed between the pixel electrode 12 and the gate line G1 of the preceding paragraph.
[0009] moreover, each source lines S1, S2, and S3 -- while having extended bending ... in the shape of a crank in the direction of Y, in order to make unnecessary the complicated color change-over circuit for supplying two or more chrominance signals to the suitable timing for the same source line, to the same source line, only the pixel electrode 12 of the pixel field corresponding to the same color is connected through TFT11. Therefore, the pixel field corresponding to the same color will be arranged by turns on both sides of a source line for every step at the same source line. for example, the pixel fields P12, P22, and P32 which corresponded green in the case of the source line S2 ... is arranged by turns at the both sides of the source line S2. Moreover, the physical relationship of TFT11 and a source line is also reverse for every step inevitably.
[0010] consequently, the gate lines G1 and G2 and G3 -- each pixel fields P11, P12, and P13 located in a line in the direction of X along with ... between ... While the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS (the 1st polar zone C1 and 2nd polar zone C2) is the same Pixel fields P12, P22, and P32 located in a line in the direction of Y along with the source line S2 ... In between, the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS has relation of bilateral symmetry for every step. for example, the pixel fields P11, P12, and P13 linked to the gate line G1 -- the pixel fields P21, P22, and P23 linked to the ... and gate line G2 -- between ..., the relative physical relationship of TFT11, the pixel electrode 12, and the retention volume capacitor CS is bilateral symmetry.
[0011] Such a manufacture approach of the active-matrix substrate of a configuration is briefly explained with reference to drawing 15 . Drawing 15 (A), (B), and (C) are the I-I' sectional view of drawing 14 , an II-II' sectional view, and an III-III' sectional view, respectively. In drawing 15 (A), first, after forming a polycrystalline silicon thin film on a substrate 10, the polycrystalline silicon thin film 110 which constitutes the active region of TFT11 and the 1st polar zone C1 of the retention volume capacitor CS is formed by patterning by the photolithography technique. Next, gate oxide 114 and the dielectric film C3 of the retention volume capacitor CS are formed by thermal oxidation of the polycrystalline silicon film 110. Next, only to the polycrystalline silicon film 110 for constituting the retention volume capacitor CS, an impurity is doped selectively and the 1st polar zone C1 of the retention volume capacitor CS is formed. Then, the gate electrode 113 and the 2nd polar zone C2 of the retention volume capacitor CS are formed with the doped silicon film of polycrystal by the

photolithography technique. It is in the condition that the gate electrode 113 and the gate line G2 were connected electrically, and the 2nd polar zone C2 and the gate line G1 of the preceding paragraph were electrically connected in the pixel field P21 by this condition.
[0012] Next, the source field 111 and the drain field 112 are formed by driving in ion by using the gate electrode 113 as a mask. Next, a through hole is formed in it after forming an interlayer insulation film 115.
[0013] The source terminal 118 and the drain terminal 119 are electrically connected to after an appropriate time to the source field 111 and the drain field 112, respectively. Here, the source terminal 118 is electrically connected to the source line S1, and the drain terminal 119 is electrically connected to the pixel electrode 12.
[0014] Thus, while forming TFT11 and the retention volume capacitor CS in the pixel field P21, as shown in drawing 15 (B) and (C), the retention volume capacitor CS is formed also in the pixel fields P11, P12, and P22.
[0015] however, each pixel fields P12, P22, and P32 which will be located in a line in the direction of Y along with the source line S2, for example if a gap of alignment occurs in a longitudinal direction (the direction of X) when the pattern shown in drawing 14 is used, and forming each component with the photolithography technique on the substrate 10 -- in ..., structure parameters will differ for every step.
[0016] Namely, the formation pattern A1 of the polycrystalline silicon film by the side of the lower layer for forming the 1st polar zone C1 of TFT11 and the retention volume capacitor CS in drawing 16 , the gate lines G1 and G2 and G3 -- with the formation pattern A2 of the polycrystalline silicon film by the side of the upper layer for forming the 2nd polar zone C2 of ..., the gate electrode 113, and the retention volume capacitor CS When a slash is attached for a ******** part as an opposite part C0 of the retention volume capacitor CS, If alignment shifts to right and left between the formation pattern A1 of the polycrystalline silicon film by the side of a lower layer, and the formation pattern A2 of the polycrystalline silicon film by the side of the upper layer the gate line G1 and G3 -- the pixel fields P11 and P12 of the odd level eye chosen by ... ... P31 and P32 -- the retention volume capacitor CS of ... (ODD) (it connects with ... these retention volume capacitors -- the gate lines G0 and G2 --) The gate line G2, pixel fields P21 and P22 chosen by ... (G4) ... Retention volume capacitor CS (EVEN) (these retention volume capacitors) the gate line G1 and G3 -- it connects with ... In between, the area of the opposite part C0 which attached the slash is changed. Since the ideal case where there is no gap of alignment in a longitudinal direction is shown in drawing 16 , the capacity value of the retention volume capacitor CS (ODD) and the capacity value of the retention volume capacitor CS (EVEN) are equal to it.

[0017] However, when a gap of alignment is in a longitudinal direction, it has a different value from the capacity value of the retention volume capacitor CS (ODD), and the capacity value of the retention volume capacitor CS (EVEN). For example, if formed in the condition that the formation pattern A1 of the polycrystalline silicon thin film by the side of a lower layer shifted in the direction of an arrow head R to the formation pattern A2 of the polycrystalline silicon thin film by the side of the upper layer, the capacity value of the retention volume capacitor CS (EVEN) will become small to the capacity value of the retention volume capacitor CS (ODD) becoming large.
[0018] consequently -- the case where TFT of N type is used -- the gate line G1 of an odd level eye, and G3 -- the optimal LC common electrical potential difference of ... the gate line G2 of an even level eye -- the problem that become higher than the optimal LC common electrical potential difference of ..., a difference occurs on an optimal LC common electrical potential difference, and a flicker occurs per gate line arises.
[0019]
[Means for Solving the Problem] In order to cancel such a trouble, the object of this invention is to offer a active-matrix substrate without a flicker, even when the pixel electrode of each pixel field connects from a left dextrotorsion pair side by turns for every step to the same source line by improving the formation pattern of each polar zone which constitutes a retention volume capacitor. Moreover, another object of this invention is to offer the quality color liquid crystal display using the active-matrix

substrate constituted in this way.
[0020] In order to solve such a technical problem, with the 1st gestalt of this invention First, two or more gate lines prolonged in the direction of X to the active-matrix substrate, Two or more pixel electrodes arranged corresponding to the intersection of two or more source lines prolonged in the direction of Y which intersects perpendicularly with the direction of X, and said gate line and said source line, Two or more thin film transistors which have the drain field electrically connected to the source field electrically connected to the gate electrode electrically connected to said gate line, and said source line, and said pixel electrode, and have been arranged corresponding to said pixel electrode, Two or more retention volume capacitors which have the 1st polar zone electrically connected to said pixel electrode and the 2nd polar zone electrically connected to the gate line of the preceding paragraph, and have been arranged corresponding to said pixel electrode are formed.
[0021] and about the pixel electrodes which adjoin each other in the direction of Y among two or more pixel electrodes electrically connected through said thin film transistor to the same source line While arranging so that it may be located in an opposite hand on both sides of said same source line, it has the description to make the same the relative formation location of said 1st polar zone to said 2nd polar zone among the retention volume capacitors electrically connected to the adjoining gate line. With the 2nd gestalt of this invention, a active-matrix substrate is received first. Two or more gate lines prolonged in the direction of X, and two or more retention volume lines prolonged in the direction of X, Two or more pixel electrodes arranged corresponding to the intersection of two or more source lines prolonged in the direction of Y which intersects perpendicularly with the direction of X, and said gate line and said source line, Two or more thin film transistors which have the drain field electrically connected to the source field electrically connected to the gate electrode electrically connected to said gate line, and said source line, and said pixel electrode, and have been arranged corresponding to said pixel electrode, The retention volume capacitor which has the 1st polar zone electrically connected to said pixel electrode and the 2nd polar zone electrically connected to said retention volume line, and has been arranged corresponding to said pixel electrode is formed.
[0022] and about the pixel electrodes which adjoin each other in the direction of Y among two or more pixel electrodes electrically connected through said thin film transistor to the same source line While arranging so that it may be located in an opposite hand on both sides of said same source line, it is characterized by making the same the relative formation location of said 1st polar zone to said 2nd polar zone among the retention volume capacitors electrically connected to the adjoining retention volume line.
[0023] thus, in the constituted active-matrix substrate Since the relative formation location of said 1st polar zone to said 2nd polar zone is the same among the retention volume capacitors which adjoin in the direction of Y, When forming each component using a photolithography technique, even if a gap of alignment occurs, among those retention volume capacitors A difference does not occur to the opposed face product of the 1st polar zone and the 2nd polar zone, but capacity value of those retention volume capacitors can be made into homogeneity.
[0024] So, generating of the flicker in the gate line unit by a retention volume value being different between adjoining retention volume capacitors can be prevented by using the active-matrix substrate of such a configuration for a liquid crystal display.
[0025] In this invention, in constituting the color liquid crystal display of a delta array using the aforementioned active-matrix substrate First, the 1st light filter train by which the light filter of the red formed corresponding to the pixel electrode and three green and blue colors was periodically arranged in the direction of X by making the three aforementioned colors into one unit, The 2nd light filter train which adjoined this 1st light filter train in the direction of Y, and was periodically arranged in the direction of X by making the three aforementioned colors into one unit is established. And while arranging the 1st light filter train and the 2nd light filter train in the condition that only the distance equivalent to 1/[of the 1 aforementioned unit period] 2 period shifted in the direction of X by turns, to the same source line, only the pixel electrode corresponding to the light filter of the same color is connected.

[0026] Moreover, in this invention, in constituting the color liquid crystal display of a mosaic array using the aforementioned active-matrix substrate, while arranging the 1st light filter train and the 2nd light filter train in the condition that only the distance equivalent to 1/[of the 1 aforementioned unit period] 3 period shifted in the direction of X by turns unlike the case of a delta array, to the same source line, only the pixel electrode corresponding to the light filter of the same color is connected.
[0027]
[Embodiment of the Invention] The [1st example] Drawing 1 is drawing showing the fundamental configuration of the color liquid crystal display which used the active-matrix substrate. Drawing 2 is the top view showing the formation pattern of each component of the active-matrix substrate used for the liquid crystal display of this example. In addition, as for the active-matrix substrate of this example, only the formation pattern of each component in the conventional active-matrix substrate and a pixel field is different, since other parts are the same, about the component which has a common function, the same sign is attached and the detailed explanation is omitted.
[0028] the gate lines G0, G1, and G2 prolonged in the direction of X in drawing 1 on the front face of the transparent substrate 10 which constitutes a active-matrix substrate from a color liquid crystal display of this example -- the source lines S1, S2, and S3 prolonged in the direction of ... and Y -- an intersection with ... corresponding -- the pixel fields P11, P12, and P13 ... is formed. and each pixel fields P11, P12, and P13 ... setting -- the source lines S1, S2, and S3 -- the transparent pixel electrode 12 is connected through TFT11 to ... and the gate lines G1 and G2 and G3 -- the period (selection period) whose TFT11 is an ON state by the signal from ... the liquid crystal part by volume CLC -- the source lines S1, S2, and S3 -- the picture signal supplied from ... is written in. On the other hand, the picture signal written in the liquid crystal part by volume CLC at the selection period is held at the period (non-selection period) whose TFT11 is an OFF state.
[0029] Here, in order to perform the high display of grace, it is called for that the maintenance property in a non-selection period is good. Then, gate lines G0, G1, and G2 ... Between the gate line of the preceding paragraph, and the pixel electrode 12, the retention volume capacitor CS is constituted inside. Gate lines G0, G1, and G2 ... Inside, since the gate electrode of TFT11 is not connected to the gate line G0, the gate line G0 is a capacity line of dedication substantially.
[0030] In addition, polarizing plates 41 and 42 are arranged on the outside of a substrate 10 and the opposite substrate 20.
[0031] The light filter 21 is formed in the opposite substrate 20. Generally a light filter 21 consists of the red filter R, a green filter G, and a blue filter B. Each pixel fields P11, P12, and P13 ... The pixel electrode 12 is arranged corresponding to the light filter 21 of these three colors, respectively. The array of the light filter 21 of this example is a delta array (drawing 12). Namely, the 1st light filter train F1 (light filter train of an odd level eye) by which the light filter of three colors of red (R), green (G), and blue (B) was periodically arranged in the direction of X by making these 3 color into one unit in the opposite substrate 20, The 2nd light filter train F2 (light filter train of an even level eye) which adjoined this light filter train in the direction of Y, and was periodically arranged in the direction of X by making the three aforementioned colors into one unit is formed. Only the distance in which the 1st light filter train F1 and the 2nd light filter train F2 are equivalent to 1/[of the 1 aforementioned unit period] 2 period shifts in the direction of X by turns, and it is arranged. Thus, in the constituted delta array, since each color element is distributing to homogeneity in a screen, it is suitable for especially the image display as which smooth image quality is required.
[0032] Thus, corresponding to the array of the constituted light filter, with the active-matrix substrate, as shown in drawing 2 and drawing 3 , the 1st pixel train (pixel train of an odd level eye) by which three pixel fields P11, P12, and P13 corresponding to the red filter R, the green filter G, and the blue filter B have been periodically arranged in the direction of X by making them into one unit is formed. Moreover, it is arranged so that only the distance in which the pixel fields P21, P22, and P23 which are equivalent to the same unit in the pixel train (pixel train of an even level eye) of ****** 2nd are equivalent to 1/2 period to the 1st pixel train may shift to the 1st pixel train in the direction of X in the direction of Y. Moreover, the pixel fields P31, P32, and P33 which are equivalent to the same unit in a ****** pixel

train (pixel train of an odd level eye) at the 2nd pixel train in the direction of Y are arranged so that only the distance which is equivalent to 1/2 period towards reverse to the pixel fields P21, P22, and P23 may shift. For this reason, a pixel train including the pixel fields P31, P32, and P33 is in the condition of having carried out the parallel displacement of the pixel train including the pixel fields P11, P12, and P13 in the direction of Y as it was. Therefore, each pixel fields P11, P12, and P13 ... A center position is in the condition that only the 1.5-pixel pitch shifted alternately with right and left for every step in the direction of Y.

[0033] each source lines S1, S2, and S3 -- while ... is bent in the shape of a crank -- the direction stretch ****** of Y. And only the pixel corresponding to the same color has connected to the same source line. Therefore, it has composition which only the signal for performing red and any 1 green and blue color specification should supply from the same source line. In addition, although the source line prolonged in the direction of Y was used in this example, bending in the shape of a crank instead, the source line prolonged in the direction of Y may be used, moving in a zigzag direction in the shape of a curve.

[0034] Since the fundamental configuration of any pixel field is the same, the pixel field P21 is explained to an example. Gaea ****** 113 of TFT11 is connected to the gate line G2, the source field 111 is connected to the source line S1, and the drain field 112 is connected to the pixel electrode 12 so that drawing 2 may show. The 1st polar zone C1 electrically connected to the drain field 112 and the pixel electrode 12 is formed in the pixel field P21, and the 1st polar zone C1 is formed in it by the doped silicon film. Moreover, the 2nd polar zone C1 prolonged in the direction of Y from the gate line G1 of the preceding paragraph is formed.

[0035] The 1st polar zone C1 and 2nd polar zone C2 have countered through a dielectric film, and are in the condition that the retention volume capacitor CS is formed between the gate line G2 of the preceding paragraph, and the pixel electrode 12.

[0036] thus -- the constituted active-matrix substrate -- the crank-like source lines S1, S2, and S3 ... receiving -- the pixel fields P11, P12, and P13 -- only the pixel electrode 12 of the pixel field corresponding to the same color of each light filter 21 by which the delta array was carried out among ... is connected. For this reason, pixel fields P12, P22, and P32 corresponding to [in / in the same source line S2 / the direction of Y] green (R) ... The pixel electrode 12 is connected by turns from the left dextrotorsion pair side. the other source lines S1 and S3 -- the same is said of ...

[0037] Each pixel fields P11, P12, and P13 located in a line in the direction of X along with the gate line G1 here ... In between, the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS (the 1st polar zone C1 and 2nd polar zone C2) is the same. Moreover, each pixel fields P21, P22, and P23 located in a line in the direction of X along with the gate line G2 ... Also in between, the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS (the 1st polar zone C1 and 2nd polar zone C2) is the same.

[0038] On the other hand, pixel fields P12, P22, and P32 located in a line in the direction of Y along with the source line S2 ... In between, the relative formation location of TFT11 and the pixel electrode 12 is the pattern which carries out right-and-left reversal for every step. namely, the pixel fields P11, P12, and P13 of the odd level eye linked to the gate line G1 -- the pixel fields P21, P22, and P23 of the even level eye linked to the ... and gate line G2 -- between ..., the formation pattern of TFT11 and the pixel electrode 12 is bilateral symmetry.

[0039] However, the retention volume capacitor CS is formed in the same relative position also in which pixel field. In other words, the relative position of the retention volume capacitor CS in a pixel field is the same among the retention volume capacitors which adjoin in the direction of Y.

[0040] moreover, the 1st polar zone C1 of the retention volume capacitor CS and the gate lines G0, G1, and G2 of the preceding paragraph -- the relative physical relationship between the 2nd polar zone C2 jutted out of ... each pixel fields P12, P22, and P32 -- also in which direction of the direction of X, and the direction of Y, it is the same between ...

[0041] For example, the retention volume capacitor CS is formed in the field along which the source line S1 of the preceding paragraph passes in the pixel field P12 linked to the gate line G1. The retention volume capacitor CS is formed in the field along which similarly the source line S1 of the preceding

paragraph passes also by the pixel field P32 linked to gate line G3. therefore, the gate line G1 and which pixel fields P11 and P12 linked to G3 ... P31 and P32 -- the 1st polar zone C1 of the retention volume capacitor CS has lapped with the 2nd polar zone C2 jutted [in / in ... / a stretch cage and this left-hand side field] even over the left-hand side field of the pixel electrode 12 out of the gate lines G0 and G2 of the preceding paragraph as it is from a connecting location with the drain field 112 of TFT11.
[0042] On the other hand, the retention volume capacitor CS is formed in the field along which the source line S2 which pixel field P22 self connects passes in the pixel field P22 linked to the gate line G2. therefore, which pixel fields P21 and P22 linked to the gate line G2 ... the 1st polar zone C1 of the retention volume capacitor CS -- the source field 111 from a connecting location with the drain field 112 of TFT11 -- going -- once -- turning up -- the pixel fields P11 and P12 of the odd level eye from the source field 111 neighborhood ... P31 and P32 -- it has extended even to the left-hand side field of the pixel electrode 12 like ... And in this left-hand side field, it has lapped with the 2nd polar zone C2 jutted out of the gate line G1 of the preceding paragraph (drawing 3).
[0043] Such a manufacture approach of the active-matrix substrate of a configuration is explained with reference to drawing 4 . Drawing 4 (A), (B), and (C) are the IV1IV' sectional view of drawing 2 , a V-V' sectional view, and a VI-VI' sectional view, respectively.
[0044] In drawing 4 (A), the polycrystal SHIRIKOSHI thin film 110 for forming the active region of TFT11 and the 1st polar zone C1 of the retention volume capacitor CS with a photolithography technique first on the substrate 10 which consists of quartz glass is formed.
[0045] Next, gate oxide 114 and the insulator layer C3 of the retention volume capacitor CS are formed by thermal oxidation of the polycrystalline silicon film 110. Next, the 1st polar zone C1 of the retention volume capacitor CS is formed by doping an impurity selectively only to the polycrystalline silicon film 110 for forming the retention volume capacitor CS.
[0046] Then, the gate electrode 113 and the 2nd polar zone C2 of the retention volume capacitor CS are formed from the doped silicon thin film of polycrystal with a photolithography technique. In this condition, in the pixel field P21, the gate electrode 113 is electrically connected to the gate line G2, and the 2nd polar zone C2 is in the condition of having connected with the gate line G1 of the preceding paragraph electrically.
[0047] Next, ion is driven in by using the gate electrode 113 as a mask, and the source field 111 and the drain field 112 are formed. Next, a through hole is formed in it after forming an interlayer insulation film 115.
[0048] The source terminal 118 and the drain terminal 119 are electrically connected to after an appropriate time to the source field 111 and the drain field 112, respectively. Here, the source terminal 118 is electrically connected to the source line S1, and the drain terminal 119 is electrically connected to the pixel electrode 12.
[0049] Thus, while forming TFT11 and the retention volume capacitor CS in the pixel field P21, as shown in drawing 4 (B) and (C), the retention volume capacitor CS is formed also in the pixel fields P11, P12, and P22.
[0050] when forming each component on the substrate 10 with the photolithography technique, even if a gap of the alignment of a pattern mask occurs in a longitudinal direction (the direction of X) in such a manufacture approach -- this example -- each pixel fields P11, P12, and P13 -- in ..., structure parameters do not differ for every step Namely, formation pattern A3 of the polycrystalline silicon film by the side of the lower layer for forming the 1st polar zone C1 of TFT11 and the retention volume capacitor CS in drawing 5 , the gate lines G1 and G2 and G3, when a slash is attached and a lap part with formation Bataan A4 of the polycrystalline silicon film by the side of the upper layer for forming the 2nd polar zone C2 of ..., the gate electrode 113, and the retention volume capacitor CS is expressed as an opposite part C0 of the retention volume capacitor CS Even if alignment shifts in the direction of X between formation pattern A3 of the polycrystalline silicon film, and formation pattern A4 of the polycrystalline silicon film the gate line G1 and G3 -- the pixel fields P11 and P12 linked to ... ... P31 and P32 -- the retention volume capacitor CS (ODD) of ... (pixel field of an odd level eye) (it connects with ... these retention volume capacitors -- the gate lines G0 and G2 and G3 --) the gate line G2 -- the

pixel fields P21 and P22 linked to ... the retention volume capacitor CS (EVEN) of ... (pixel field of an even level eye) (these retention volume capacitors) the gate line G1, G3, and G5 -- it connects with ... The area of the opposite part C0 is not changed in between.
[0051] For example, even if formed in the condition that formation pattern A3 of a polycrystalline silicon thin film shifted in the direction of an arrow head R a little to formation Bataan A4 of a polycrystalline silicon thin film the pixel fields P11 and P12 of an odd level eye ... P31 and P32 -- the pixel fields P21 and P22 of ... and an even level eye -- in the both sides of ..., the area of the opposite part C0 of the 1st polar zone C1 and the 2nd polar zone C2 in each retention volume capacitor CS only becomes small. On the contrary, even if formed in the condition that formation Bataan A3 of a polycrystalline silicon thin film shifted in the direction of an arrow head L a little to formation pattern A4 of a polycrystalline silicon thin film the pixel fields P11 and P12 of an odd level eye ... P31 and P32 -- the pixel fields P21 and P22 of ... and an even level eye -- in the both sides of ..., the area of the opposite part C0 of the 1st polar zone C1 and the 2nd polar zone C2 in each retention volume capacitor CS only becomes large.
[0052] Moreover, even if alignment shifts to up down (the direction of Y) one somewhat, the area of the opposite part C0 of the 1st polar zone C1 and the 2nd polar zone C2 in each retention volume capacitor CS does not change.
[0053] thus, in the active-matrix substrate of this example Even if alignment shifts in a longitudinal direction (the direction of X), or the vertical direction (the direction of Y) between formation pattern A3 of the polycrystalline silicon film, and formation pattern A4 of the polycrystalline silicon film Each pixel fields P11 and P12 ... P21, P22 ... P31, P32 ... In between Since the capacity value of each retention volume capacitor CS is always equal, they are the gate line G1 of an odd level eye, and G3... The optimal LC common electrical potential difference, and the gate line G2 of an even level eye and the optimal LC common electrical potential difference of .. are always the same. So, since an overall optimal LC common electrical potential difference can be set up, the flicker in a gate line unit can be prevented.
[0054] furthermore, the pixel fields P11, P12, and P13 located in a line in the direction of Y along with the source lines S1, S2, and S3 in this example -- right-and-left reversal of the relative formation location of TFT11 and the pixel electrode 12 is only carried out for every step between ..., and the 1st formation location and configuration of the polar zone C1 for forming the retention volume capacitor CS only differ from each other. Therefore, the flicker which originates in the alignment gap at the time of forming the 1st polar zone C1 and 2nd polar zone C2 only by optimizing the relative physical relationship of the 1st polar zone C1 and the 2nd polar zone C2 is prevented. So, since it can apply also when the formation field and magnitude of each component have a limit, it is advantageous, highly minute and especially in case the liquid crystal display of high density is realized.
[0055] moreover, the gate line G1 of an odd level eye and G3 -- the pixel fields P11 and P12 corresponding to ... the gate line G2 of a ... and even level eye -- the pixel fields P21 and P22 corresponding to ... the pattern of components other than the 1st polar-zone C1 is substantially the same between ... so -- even if the alignment gap with the opposite substrate 20 and a active-matrix substrate or the ally AMENTO gap on a active-matrix substrate occurs -- the gate line G1 of an odd level eye, and G3 -- the pixel fields P11 and P12 corresponding to ... the gate line G2 of a ... and even level eye -- the pixel fields P21 and P22 corresponding to ... between ..., the difference of a numerical aperture is also mitigated and the horizontal line unevenness by it can also be prevented.
[0056] The [2nd example] Drawing 6 is the top view showing the formation pattern of each component of the AKUIBU matrix substrate of the liquid crystal display of this example. In addition, only the part of a retention volume capacitor is different from the active-matrix substrate concerning the 1st example, and since other parts are the same, the active-matrix substrate of this example has given the same sign to the component which has the function to correspond.
[0057] Although it was the structure of using the gate line of the preceding paragraph in the 1st example although the 2nd polar zone C2 of each retention volume capacitor CS is formed this example -- the retention volume lines CM1, CM2, and CM3 of constant potential ... the gate lines G1 and G2 and G3 --

it forms in the condition of having extended in the direction of X in ... and juxtaposition -- having -- the retention volume capacitor CS -- the retention volume lines CM1, CM2, and CM3 -- the 2nd polar zone C2 is constituted using ...
[0058] In addition, red and three each pixel fields P21, P22, and P23 which correspond green and blue are periodically arranged in the direction of X by making them into one unit with the liquid crystal display of this example as well as the 1st example. Moreover, also in the pixel train which adjoins in the direction of Y, the pixel fields P11, P12, and P13 and the pixel fields P31, P32, and P33 which are similarly equivalent to one unit shift 1/2 period at a time alternately with right and left, and are arranged.

[0059] here -- each source lines S1, S2, and S3 ... is formed in the shape of a crank. Moreover, to the same source line, only the pixel electrode of the pixel field corresponding to the same color has connected. Therefore, it has composition which only the signal for performing red and any 1 green and blue color specification should supply from the same source line.
[0060] Moreover, someday, since the fundamental configuration of ******** is the same, if the pixel field P21 is explained to an example, the 1st polar zone C1 which consists of doped silicon film electrically connected to the drain field 112 and the pixel electrode 12 is formed in the pixel field P21, and the 2nd polar zone C2 prolonged in the direction of Y is formed in it from the retention volume line CM 2. The 1st polar zone C1 and the 2nd polar zone C2 have countered through a dielectric film, and the retention volume capacitor CS consists of pixel fields P21 between the pixel electrode 12 and the retention volume line CM 2.
[0061] Thus, pixel fields P11, P12, and P13 corresponding to the same color of each light filter 21 by which the delta array was carried out to the crank-like source line in the constituted active-matrix substrate ... Only the pixel electrode 12 was connected and the pixel electrode 12 of the pixel fields P12, P22, and P32 has connected from the left dextrotorsion pair side to the same lease line S2. the other source lines S1 and S3 -- the same is said of ...
[0062] Therefore, each pixel fields P11, P12, and P13 located in a line in the direction of X like the 1st example ... In between While the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS (the 1st polar zone C1 and 2nd polar zone C2) is the same, it sets in the direction of Y. the pixel fields P12, P22, and P32 -- the relative formation location of the TFT11 and the pixel electrode 12 in ... is carrying out right-and-left reversal for every step.
[0063] However, the retention volume capacitor CS is formed in the same relative position also in which pixel field. In other words, it is the same among the retention volume capacitors which adjoin in the relative position of the retention volume capacitor CS in a pixel field, and the direction of Y.
[0064] moreover, the 1st polar zone C1 of the retention volume capacitor CS and the retention volume lines CM1 and CM2 -- the relative physical relationship between the 2nd polar zone C2 jutted out of ... is the same among the retention volume capacitors which adjoin in the direction of Y. That is, it is the same between each pixel field.
[0065] such a manufacture approach of the active-matrix substrate of a configuration -- the 1st example -- almost -- the same -- the gate electrode 113, the gate lines G1 and G2, and G3 -- the time of forming ... the retention volume lines CM1, CM2, and CM3 -- only the point which forms simultaneously the 2nd polar zone C2 jutted out of ... and them is different.
[0066] Therefore, formation pattern A3 of the polycrystalline silicon film by the side of the lower layer for forming the 1st polar zone C1 of TFT11 and the retention volume capacitor CS in drawing 7 , the gate lines G1 and G2 and G3 ... the gate electrode 113 and the retention volume lines CM1, CM2, and CM3, when a slash is attached and a lap part with formation pattern A5 of the polycrystalline silicon film by the side of the upper layer for forming the 2nd polar zone C2 of ... and the retention volume capacitor CS is expressed as an opposite part C0 of the retention volume capacitor CS Even if alignment shifts to a longitudinal direction (the direction of X) between formation pattern A3 of the polycrystalline silicon film, and formation pattern A5 of the polycrystalline silicon film, they are each pixel fields P11 and P12... P21, P22 ... P31, P32 ... In between The area (capacity value of the retention volume capacitor CS) of the opposite part C0 which attached the slash always becomes equal. So, according to this

example, it has the same effectiveness as the 1st example -- the flicker in a gate line unit can be prevented.
[0067] The [3rd example] In the 1st and 2nd examples, as a switching element, it replaces with this and each has used TFT of a reverse stagger mold by this example, although TFT of a coplanar mold was used.
[0068] Drawing 8 is the sectional view of TFT which used the amorphous silicon film for the active layer, and a retention volume capacitor. In drawing 8 , gate electrode 113A which consists of tantalum film on substrate film 110A is formed in the front-face side of glass substrate 10A, and tantalic acid ghost 114A as gate dielectric film is formed in the front face. Silicon nitride 114B is formed in the front face of tantalic acid ghost 114A, and tantalic acid ghost 114A and silicon nitride 114B function on it as gate dielectric film. Intrinsic amorphous silicon film 117A for forming a channel is formed in the front-face side of silicon nitride 114B. Amorphous silicon film 116A of high-concentration N type is formed in the front-face side of intrinsic amorphous silicon film 117A. The part set to gate electrode 113A at the time of a pair is etched, and amorphous silicon film 116A of N type is divided into source field 111A and drain field 112A. aluminum electrode layer 118B forms in source field 111A through molybdenum layer 118A -- having -- **** -- this aluminum electrode layer 118B -- the source lines S1, S2, and S3 -- it connects with ... Pixel electrode 12A which consists of ITO film is connected to drain field 112A.
[0069] Pixel electrode 12A (ITO film) is the pixel fields P11, P12, and P13, as shown in drawing 9 ... It is formed even in the edge and the edge of pixel electrode 12A is the 1st polar zone C1 of the retention volume capacitor CS there.
[0070] The dielectric film C3 of the retention volume capacitor CS which consists of gate dielectric film, tantalic acid ghost 114A formed in coincidence, and silicon nitride 114B is formed in the lower layer side of the 1st polar zone C1. The tantalum film formed simultaneously with gate electrode 113A is formed in the lower layer side of a dielectric film C3, and this tantalum film has become the 2nd polar zone C2 of the retention volume capacitor CS. Since it has become same the 1st example and omitting other configurations, the detailed explanation is omitted. this example also shows to drawing 9 -- as -- the pixel fields P11, P12, and P13 ... is arranged corresponding to the light filter 21 of a delta array. the source lines S1, S2, and S3 same here -- the pixel fields P11, P12, and P13 corresponding to the same color to ... only pixel electrode 12A of ... is connected. for this reason, the pixel fields P12, P22, and P32 corresponding to green (R) in the same source line S2 ... has connected by turns from the left dextrotorsion pair side of the source line S2.
[0071] even in this case, the pixel fields P12, P22, and P32 located in a line in the direction of Y along with the source line S2 like the 1st example -- in ..., the formation location of the retention volume capacitor CS is located in the same location in a pixel field. Namely, although the 1st polar zone C1 of the retention volume capacitor CS is different from an example 1 at the point which consists of edges of pixel electrode 12A this 1st polar zone C1 and the gate of the preceding paragraph -- green -- G0, G1, and G2 -- the relative physical relationship between the 2nd polar zone C2 jutted out of ... the pixel fields P11, P12, and P13 -- it is set up so that it may be in agreement also in which direction of the direction of X, and the direction of Y between ... So, formation PA evening-N A7 of the ITO film for forming the 1st polar zone C1 of pixel electrode 12A and the retention volume capacitor CS in drawing 10 , the gate lines G1 and G2 and G3, when a slash is attached and a lap part with the formation pattern A6 of the Than evening RU film for forming the 2nd polar zone C2 of ..., gate electrode 113A, and the retention volume capacitor CS is expressed as an opposite part C0 of the retention volume capacitor CS In case the formation pattern A7 of the ITO film and the formation pattern A6 of the tantalum film are formed, even if an alignment gap occurs in a longitudinal direction (the direction of X) the gate line G1 of an odd level eye, and G3 -- the pixel fields P11 and P12 linked to ... ... P31 and P32 -- with the retention volume capacitor CS of ... the gate line G2 -- the pixel fields P21 and P22 linked to ... between the retention volume capacitors CS of ..., the area (capacity value of the retention volume capacitor CS) of the opposite part C0 which attached the slash is equal. So, according to this example, it has the same effectiveness as the 1st example -- generating of the flicker in a gate line unit can be prevented.
[0072] in addition -- this example -- the 2nd polar zone C2 -- forming -- hitting -- the 1st example -- the

same -- the gate lines G0, Gl, and G2 of the preceding paragraph, and G3 -- although ... was used -- the 2nd example -- like -- the retention volume lines CMl, CM2, and CM3 of dedication ... may be formed and the retention volume capacitor CS may be constituted using it.
[0073] The [4th example] Although the 1st thru/or the 3rd example are examples about the liquid crystal display which used the light filter of a delta array, this example is an example about the liquid crystal display which used the light filter of a mosaic array. In addition, in this example, since the light filter is a mosaic array, the pixel is arranged in the shape of a grid, but since it is the same as that of the 1st example, other parts give the same sign to a corresponding part, and omit those detailed explanation.
[0074] Drawing 11 is drawing having shown the pattern of each component of the active-matrix substrate of this example. the gate lines G1 and G2 prolonged in the direction of X in the front face of a transparent substrate, and G3 -- the source lines S1, S2, and S3 prolonged in the direction of ... and Y -- an intersection with ... corresponding -- the pixel fields P11, P12, and P13 ... is formed. these pixel fields P11, P12, and Pl3 ... the source lines S1, S2, and S3 -- the transparent pixel electrode 12 is connected through TFT11 as a switching element to ... in order [moreover,] to improve the maintenance property in the liquid crystal part by volume CLC -- the gate lines G0, G1, and G2 of the preceding paragraph, and G3 -- the retention volume capacitor CS is formed between the ... and pixel electrodes 12.
[0075] although such a configuration is the same as the case where a light filter 21 is a delta array, like the 1st thru/or the 3rd example, since the light filter 21 of red R, Green G, and blue B is formed in the mosaic array, by this example, it corresponds to the light filter 21 of red R, Green G, and blue B -- as -- the pixel fields P11, P12, and P13 ... is arranged. drawing 11 -- each pixel fields P11, P12, and P13 -- it has shown the class of color of the light filter corresponding to ... by (R), (G), and (B). Here, the light filter of red and three green and blue colors is periodically arranged in the direction of X by making these 3 color into one unit, as shown in drawing 13 . Here, the 1st light filter train F1 (light filter train of an odd level eye) and 2nd light filter train F2' (light filter train of an even level eye) are in the condition that only the distance equivalent to 1/[of the 1 aforementioned unit period] 3 period shifted in the direction of X by turns.
[0076] the pixel fields P11, P12, and P13 connected to the gate line G1 corresponding to the array of such a light filter -- by making three pixel fields Pll, P12, and P13 corresponding to the light filter 21 of red R, Green G, and blue B at ... into one unit, it is arranged repeatedly linearly and the 1st pixel train (pixel train of an odd level eye) is formed in the direction of X. moreover, the pixel fields P21, P22, and P23 linked to the gate line G2 -- it is linearly arranged [in the 2nd pixel train (pixel train of an even level eye) which consists of ...] repeatedly in the direction of X by making three pixel fields P21, P22, and P23 corresponding to red R, Green G, and blue B into one unit. the distance which is equivalent to 1/3 period when arranging periodically as one unit the pixel field of red R, Green G, and three colors corresponding to the light filter 21 of blue B here between the 1st pixel train (pixel train of an odd level eye), and the 2nd pixel train (pixel train of an even level eye) -- the direction of X -- and it is arranged so that it may shift by turns. Consequently, each pixel fields P11, P12, and P13 ... A center position In the AKUIBU matrix substrate in the condition that only the l pixel pitch shifted alternately with right and left for every step constituted in this way a delta array -- being different -- each source lines S1, S2, and S3 -- the case where only the pixel electrode of the pixel field corresponding to the same color connects to the same source line among ... the source lines S1, S2, and S3 -- it is formed so that ... may be linearly prolonged in between each pixel field toward the direction of Y.
[0077] Here, they are the pixel fields P12, P22, and P32 in the same source line S2, for example, the source... It is the same as that of the 1st thru/or the 3rd example that the pixel electrode 12 is connected by turns from a left dextrotorsion pair side. Therefore, each pixel fields P11, P12, and P13 located in a line in the direction of X ... Although the relative formation location of TFT11, the pixel electrode 12, and the retention volume capacitor CS (the 1st polar zone C1 and 2nd polar zone C2) is the same in between Pixel fields P12, P22, and P32 which are cured on the source line S2 and located in a line in the direction of Y ... In between, the relative formation location of TFT11 and the pixel electrode 12 is right and left reversed for every step.
[0078] However, the retention volume capacitor CS is formed in the same relative position also in which

pixel field. In other words, the relative position of the retention volume capacitor CS in a pixel field is the same among the retention volume capacitors which adjoin in the direction of Y.
[0079] moreover, the 1st polar zone C1 of the retention volume capacitor CS and the gate lines G0, G1, and G2 of the preceding paragraph -- the relative physical relationship between the 2nd polar zone C2 jutted out of ... each pixel fields P12, P22, and P32 -- also in which direction of the direction of X, and the direction of Y, it is the same between ... So, in case the 1st polar zone Cl of the retention volume capacitor CS and the 2nd polar zone C2 are formed the case where an alignment gap of a longitudinal direction (the direction of X) or the vertical direction (the direction of Y) occurs -- the gate line Gl of an odd level eye, and G3 -- the pixel fields P11, P12, and P13 corresponding to ... with ... the gate line G2 of an even level eye -- the pixel field P21 corresponding to ..., P22, and P23 -- since the capacity value of the retention volume capacitor CS is equal between ..., it has the same effectiveness as the 1st example -- generating of the flicker in a gate line unit can be prevented. in addition, the 1st example -- the same -- the gate lines GO, G1, and G2 of the preceding paragraph, and G3 -- although a part of ... was used for the 2nd polar zone C2 of the retention volume capacitor CS -- the 2nd example -- like -- the retention volume lines CM1, CM2, and CM3 of dedication ... may be formed and the part may be used for the 2nd polar zone C2 of the retention volume capacitor CS.
[0080] Moreover, as TFT11, TFT of a reverse stagger mold may be used not only like TFT of a coplanar mold but like the 3rd example.
[0081] [Other examples] The active-matrix substrate of this invention can prevent the flicker resulting from an alignment gap, as well as the case of a color liquid crystal display when it uses for a monochrome liquid crystal display.
[0082] Moreover, in each example, although the transparent ITO electrode was used, this invention is applicable also like the liquid crystal display of the reflective mold using the aluminum electrode etc. as a pixel electrode. Furthermore, it replaces with TFT and this invention can be applied also to the active-matrix substrate using the diode of MIM (Metal-Insulator-Metal) structure as a switching element. That is, it has same then an example 1 thru/or the same effectiveness as 4 for the relative formation location of the 1st polar zone of a retention volume capacitor, and the 2nd polar zone by the retention volume capacitors which adjoin in the direction of Y.
[0083] [Availability on industry] In this invention, it has the description as above to have made the same relative physical relationship with the pattern on top of which it can be laid if the parallel displacement of the structure of the 1st polar zone which constitutes the retention volume capacitor of a active-matrix substrate, and the 2nd polar zone is carried out between each pixel field, i.e., the 1st polar zone, and the 2nd polar zone between each pixel field. Therefore, according to this invention, in case the 1st polar zone and 2nd polar zone are formed, even if there is an alignment gap, the capacity value of a retention volume capacitor becomes equal. So, the difference of the capacity value of a retention volume capacitor can be abolished between odd gate stages and even gate stages, and a flicker can be mitigated.
[0084] Moreover, in a pixel field, although the formation location and occupancy area of the 1st polar zone and the 2nd polar zone are restricted, according to this invention, the flicker resulting from the alignment gap at the time of forming the 1st polar zone and 2nd polar zone can be prevented only by optimizing the relative physical relationship of the 1st polar zone and the 2nd polar zone. So, it is advantageous, highly minute and especially in case the liquid crystal display of high density is realized. Furthermore, between the pixel field corresponding to odd gate stages, and the pixel field corresponding to even gate stages, only the formation pattern of the 1st polar zone is different, and the pattern of other components is substantially equal. So, even if the alignment gap with an opposite substrate and a active-matrix substrate equipped with a light filter or the alignment gap on a active-matrix substrate occurs, the difference of a numerical aperture is also lost between the pixel fields linked to the pixel field and the even gate stages linked to odd gate stages, and horizontal line unevenness can be prevented effectively.

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The pixel electrodes which adjoin each other in the direction of Y among two or more pixel electrodes which were equipped with the following and were electrically connected through said thin film transistor to the same source line The active-matrix substrate which is arranged and is characterized by the relative formation location of said 1st polar zone to said 2nd polar zone being the same among the retention volume capacitors electrically connected to the adjoining gate line so that it may be located in an opposite hand on both sides of said same source line. Two or more gate lines prolonged in the direction of X Two or more source lines prolonged in the direction of Y which intersects perpendicularly with the direction of X Two or more pixel electrodes arranged corresponding to the intersection of said gate line and said source line Two or more thin film transistors which have the drain field electrically connected to the source field electrically connected to the gate electrode electrically connected to said gate line, and said source line, and said pixel electrode, and have been arranged corresponding to said pixel electrode, Two or more retention volume capacitors which have the 1st polar zone electrically connected to said pixel electrode, and the 2nd polar zone electrically connected to the gate line of the preceding paragraph, and have been arranged corresponding to said pixel electrode [Claim 2] The pixel electrodes which adjoin each other in the direction of Y among two or more pixel electrodes which were equipped with the following and were electrically connected through said thin film transistor to the same source line The active-matrix substrate which is arranged and is characterized by the relative formation location of said 1st polar zone to said 2nd polar zone being the same among the retention volume capacitors electrically connected to the adjoining retention volume line so that it may be located in an opposite hand on both sides of said same source line. Two or more gate lines prolonged in the direction of X Two or more retention volume lines prolonged in the direction of X Two or more source lines prolonged in the direction of Y which intersects perpendicularly with the direction of X Two or more pixel electrodes arranged corresponding to the intersection of said gate line and said source line, Two or more thin film transistors which have the drain field electrically connected to the source field electrically connected to the gate electrode electrically connected to said gate line, and said source line, and said pixel electrode, and have been arranged corresponding to said pixel electrode, The retention volume capacitor which has the 1st polar zone electrically connected to said pixel electrode, and the 2nd polar zone electrically connected to said retention volume line, and has been arranged corresponding to said pixel electrode
[Claim 3] It is the color liquid crystal display with which only the distance in which said 1st light filter train and said 2nd light filter train are equivalent to 1/[of the period of said one unit] 2 period is arranged at the condition of having shifted in the direction of X by turns, and is characterized by connecting only the pixel electrode corresponding to the light filter of the same color through said thin film transistor to the same source line by having the following. The 1st light filter train by which the light filter of the red which is a color liquid crystal display using the active-matrix substrate indicated by the 1st term of a claim or the 2nd term, and was formed corresponding to said pixel electrode, and three green and blue colors was periodically arranged in the direction of X by making said three colors into

one unit The 2nd light filter train which adjoined said 1st light filter train in the direction of Y, and was periodically arranged in the direction of X by making said three colors into one unit
[Claim 4] It is the color liquid crystal display with which only the distance in which said 1st light filter train and said 2nd light filter train are equivalent to 1/[of the period of said one unit] 3 period is arranged at the condition of having shifted in the direction of X by turns, and is characterized by connecting only the pixel electrode corresponding to the light filter of the same color through said thin film transistor to the same source line by having the following. The 1st light filter train by which the light filter of the red which is a color liquid crystal display using the active-matrix substrate indicated by the 1st term of a claim or the 2nd term, and was formed corresponding to said pixel electrode, and three green and blue colors was periodically arranged in the direction of X by making said three colors into one unit The 2nd light filter train which adjoined said 1st light filter train in the direction of Y, and was periodically arranged in the direction of X by making said three colors into one unit

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the fundamental configuration of the color liquid crystal display using a active-matrix substrate.
[Drawing 2] It is the top view showing the formation pattern of each component of the active-matrix substrate used for the liquid crystal display concerning the 1st example.
[Drawing 3] It is the mimetic diagram of the formation pattern shown in drawing 2 .
[Drawing 4] (A) is a sectional view in the IV-IV' line of drawing 2 , A sectional view [in / in (B) / the V-V' line of drawing 2] and (C) are the sectional views in the VI-VI' line of drawing 2 .
[Drawing 5] In the active-matrix substrate shown in drawing 2 , it is the top view showing typically the formation pattern of each silicon film which forms two polar zone of a retention volume capacitor in a substrate front face.
[Drawing 6] It is the top view showing the formation pattern of each component of the active-matrix substrate used for the liquid crystal display concerning the 2nd example.
[Drawing 7] In the active-matrix substrate shown in drawing 6 , it is the top view showing typically the formation pattern of each silicon film which forms two polar zone of a retention volume capacitor in a substrate front face.
[Drawing 8] It is the sectional view of TFT of the reverse stagger mold used as TFT of the active-matrix substrate used for the liquid crystal display concerning the 3rd example.
[Drawing 9] It is the top view showing the formation pattern of each component of the active-matrix substrate used for the liquid crystal display concerning the 3rd example.
[Drawing 10] In the active-matrix substrate shown in drawing 9 , it is the top view showing typically the formation pattern of the tantalum film which forms two polar zone of a retention volume capacitor in a substrate front face, and the ITO film.
[Drawing 11] It is the top view showing the formation pattern of each component of the active-matrix substrate used for the liquid crystal display concerning the 4th example.
[Drawing 12] It is drawing showing the color array pattern of a delta array.
[Drawing 13] It is drawing showing an example of the color array pattern of a mosaic array.
[Drawing 14] It is the top view showing the formation pattern of each component of the active-matrix substrate used for the conventional liquid crystal display.
[Drawing 15] A sectional view [in / in (A) / the I-I' line of drawing 14], a sectional view [in / in (B) / the II-II' line of drawing 14], and (C) are the sectional views in the III-III' line of drawing 14 .
[Drawing 16] In the active-matrix substrate shown in drawing 14 , it is the top view showing typically the formation pattern of each silicon film which forms two polar zone of a retention volume capacitor in a substrate front face.

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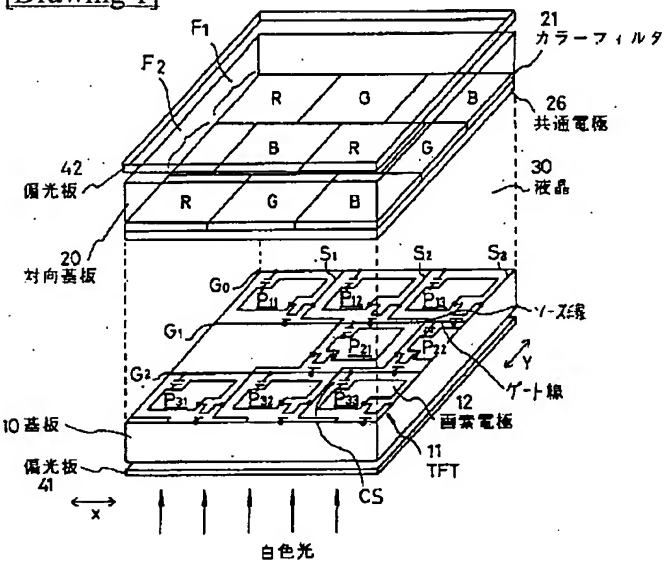
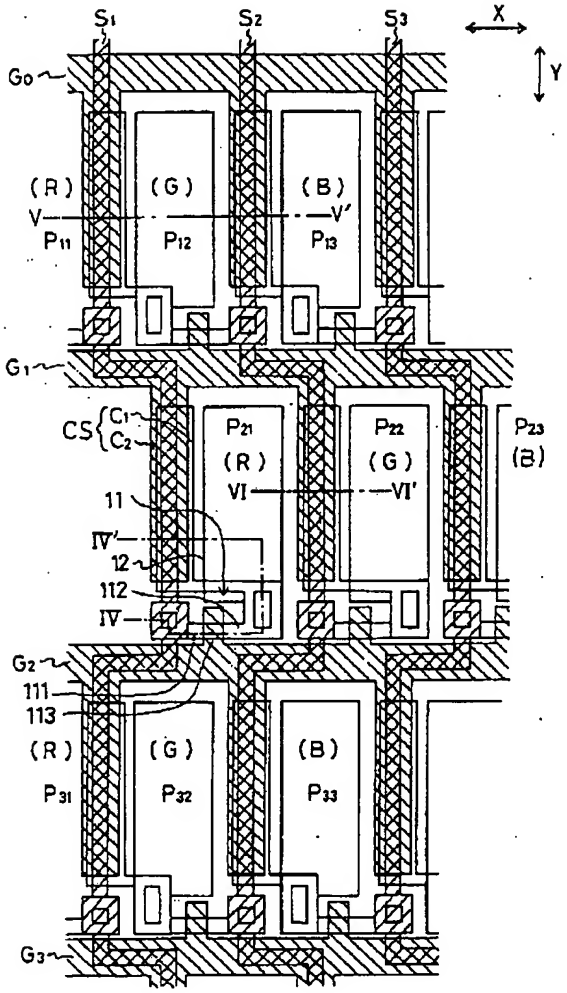
DRAWINGS

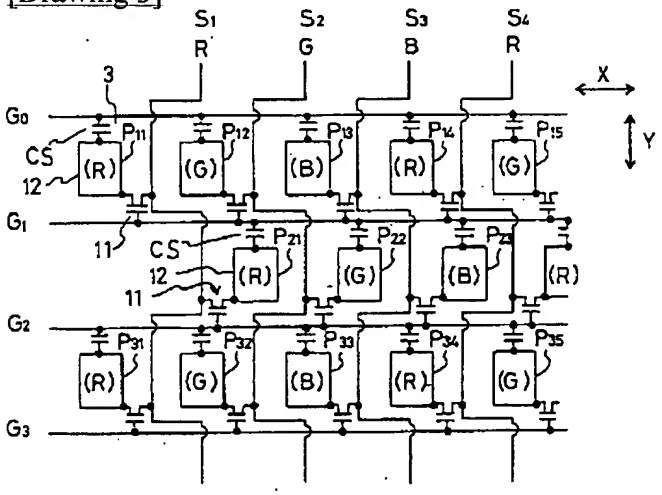
[Drawing 1]



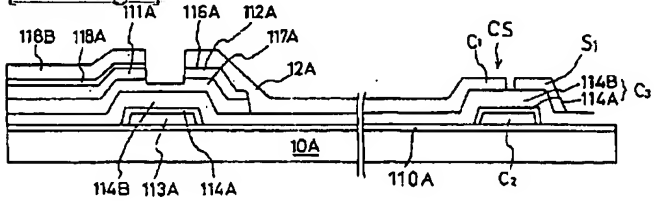
[Drawing 2]



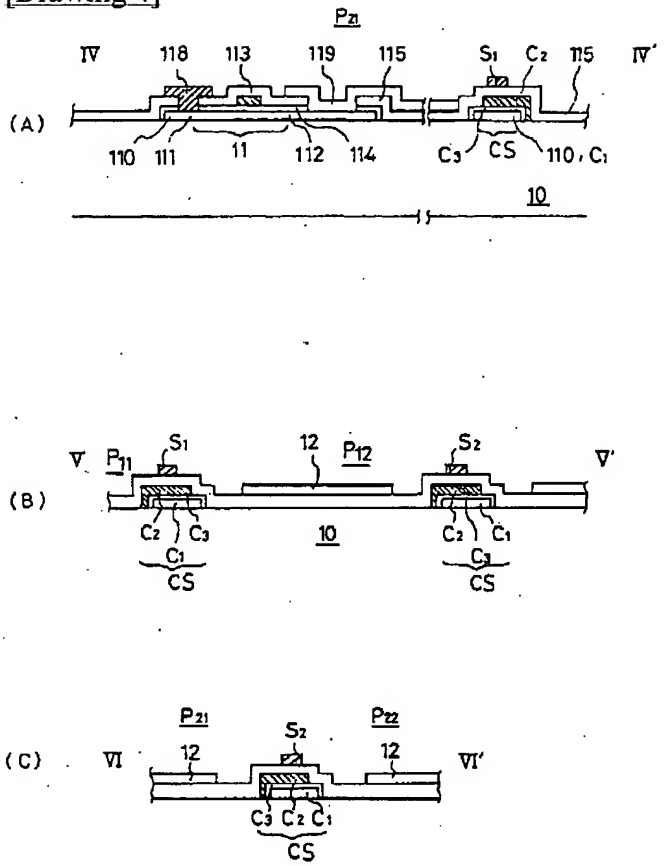
[Drawing 3]



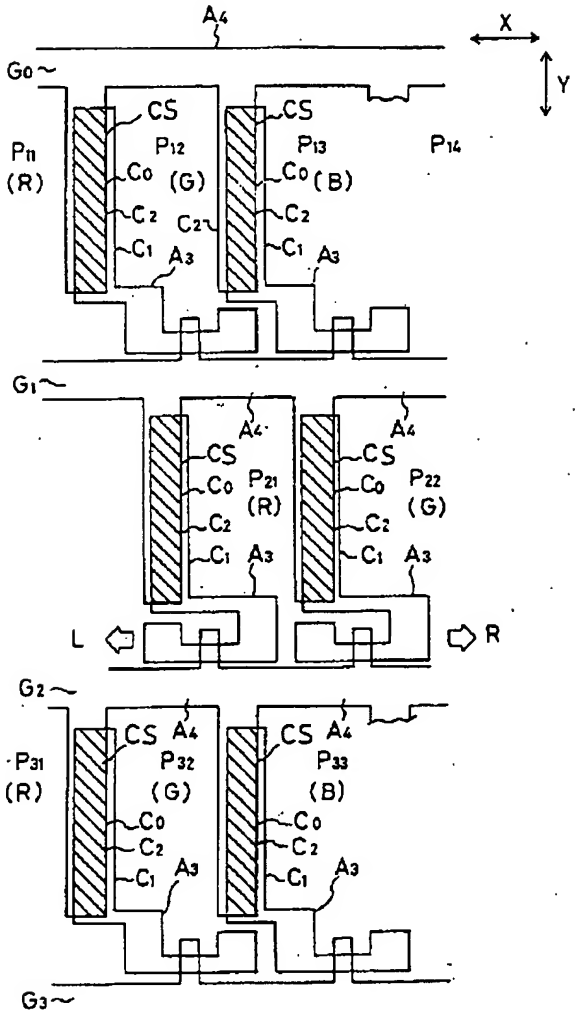
[Drawing 8]



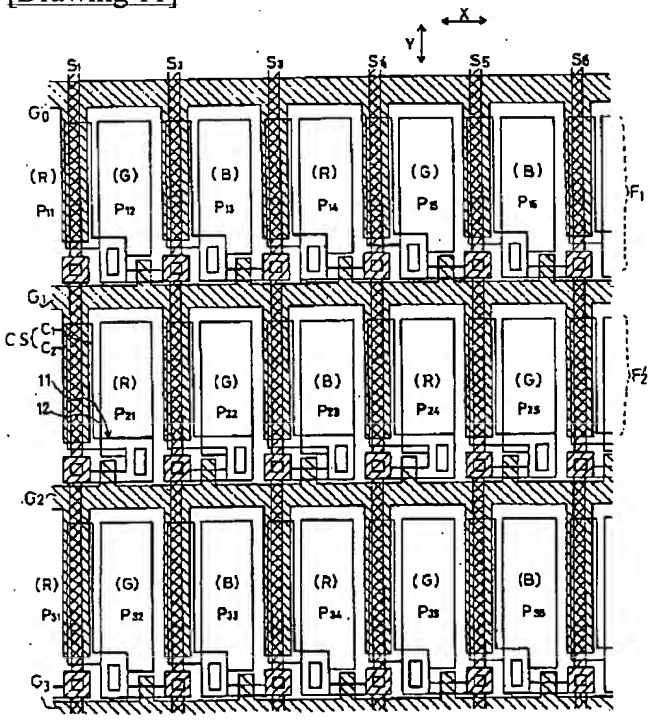
[Drawing 4]



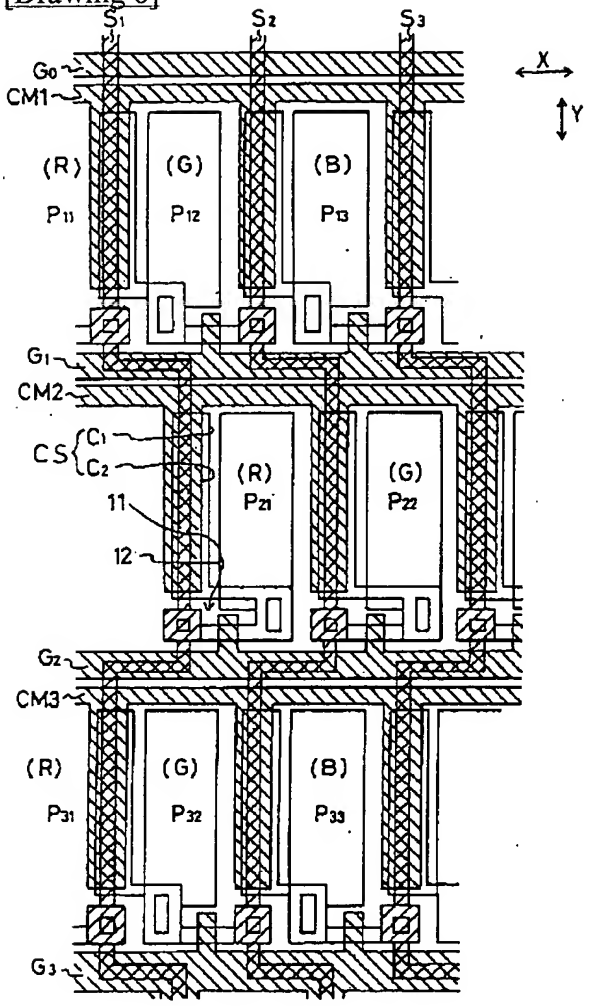
[Drawing 5]


A4
X
Y
G0
CS
P11
(R)
P12
C0
(G)
C2
C1
A3
P13
(B)
P14
G1
P21
P22
L
R
G2
P31
P32
P33
G3

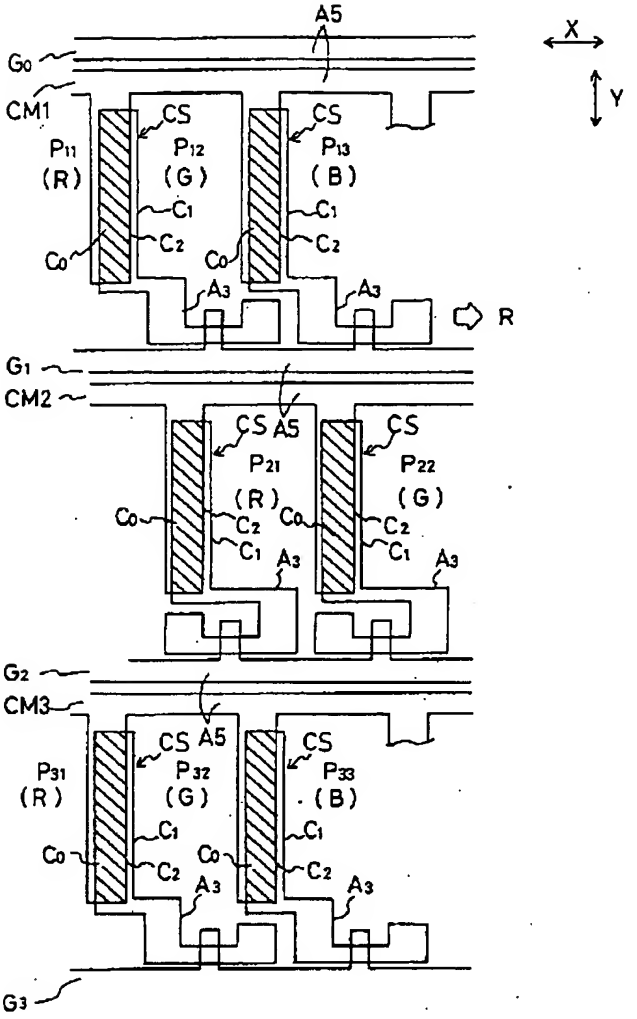
[Drawing 11]


X
Y
S1
S2
S3
S4
S5
S6
G0
(R)
(G)
(B)
P11
P12
P13
P14
P15
P16
F1
G1
CS
C1
C2
11
12
P21
P22
P23
P24
P25
F2
G2
P31
P32
P33
P34
P35
P36
G3

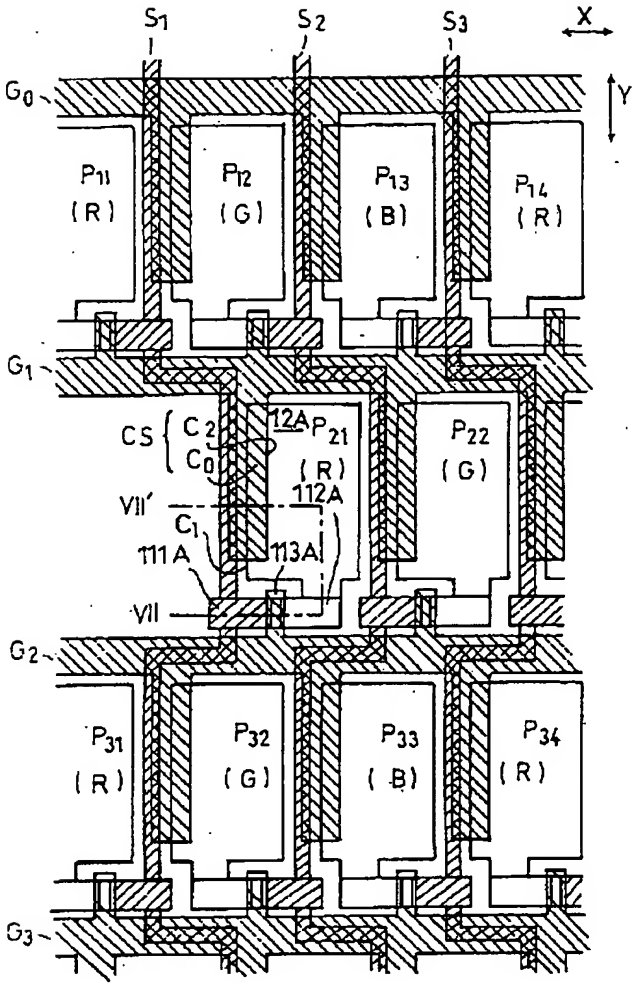
[Drawing 6]



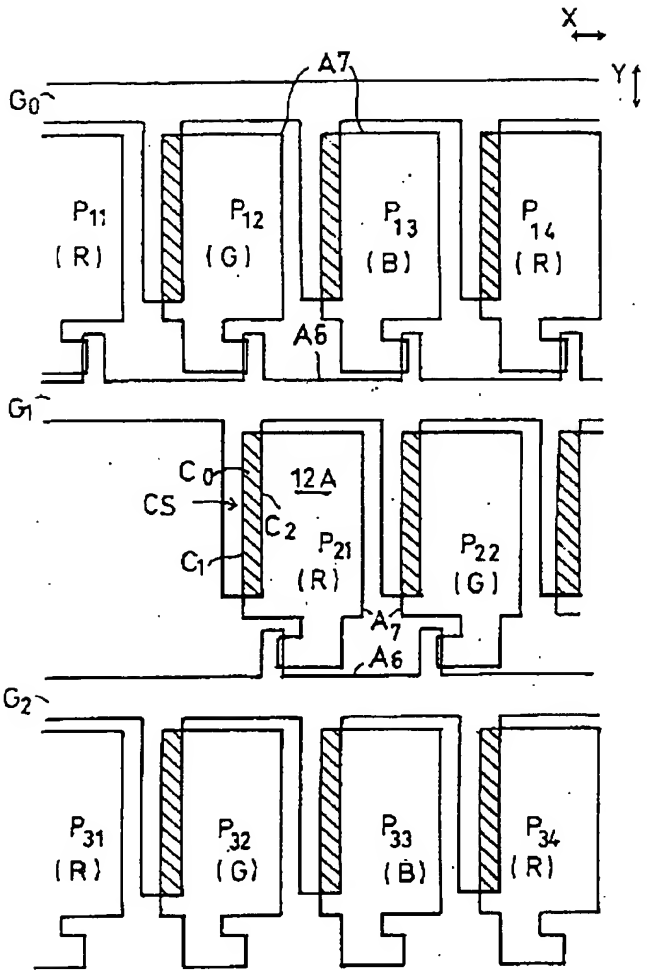
[Drawing 7]


A5
X
Y
G0
CM1
CS
P11
(R)
P12
(G)
P13
(B)
C1
C2
C0
A3
R
G1
CM2
P21
P22
G2
CM3
P31
P32
P33
G3

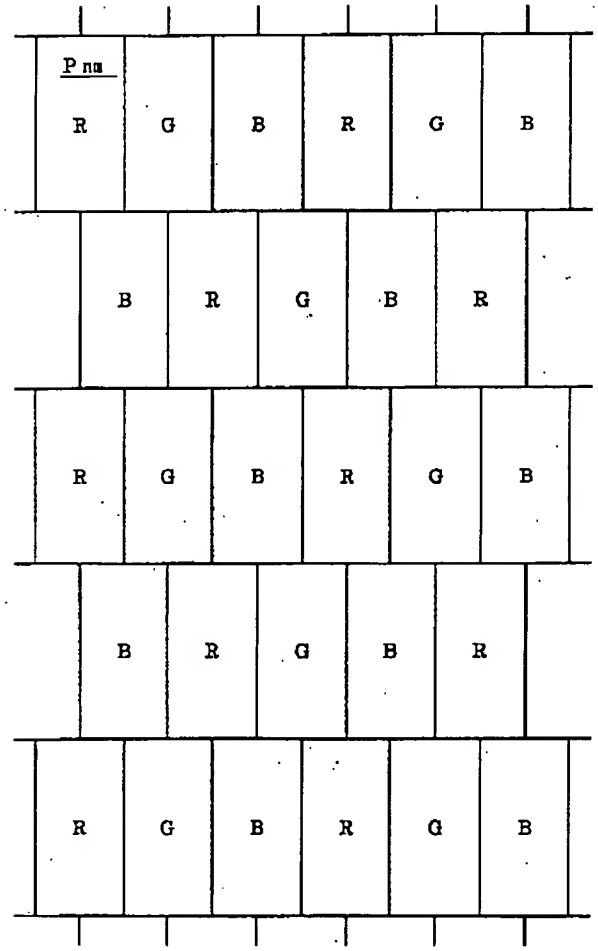
[Drawing 9]


S1
S2
S3
X
Y
G0
G1
G2
G3
P11 (R)
P12 (G)
P13 (B)
P14 (R)
CS
C2
C0
C1
12A
P21 (R)
112A
111A
113A
VII'
VII
P22 (G)
P31 (R)
P32 (G)
P33 (B)
P34 (R)

[Drawing 10]


X
Y
A7
G0
P11
(R)
P12
(G)
P13
(B)
P14
(R)
A6
G1
C0
CS
C2
C1
12A
P21
(R)
P22
(G)
A7
A6
G2
P31
(R)
P32
(G)
P33
(B)
P34
(R)

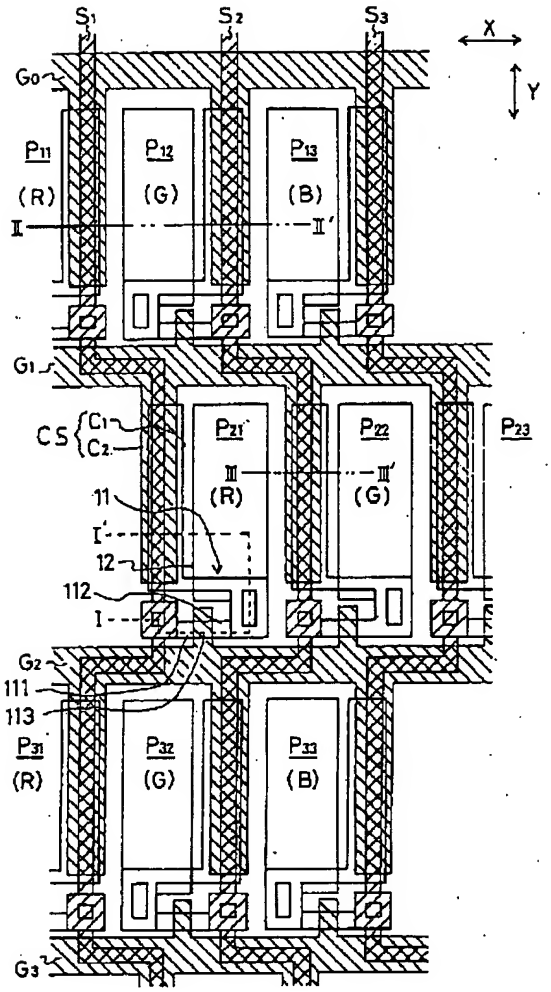
[Drawing 12]



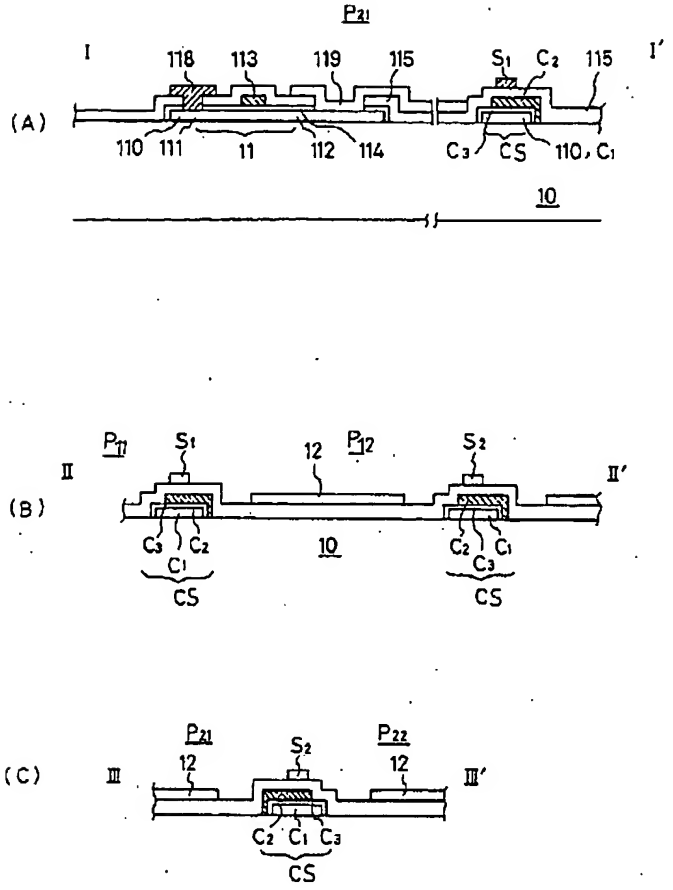
[Drawing 13]

Pnm					
R	G	B	R	G	B
B	R	G	B	R	G
R	G	B	R	G	B
B	R	G	B	R	G
R	G	B	R	G	B

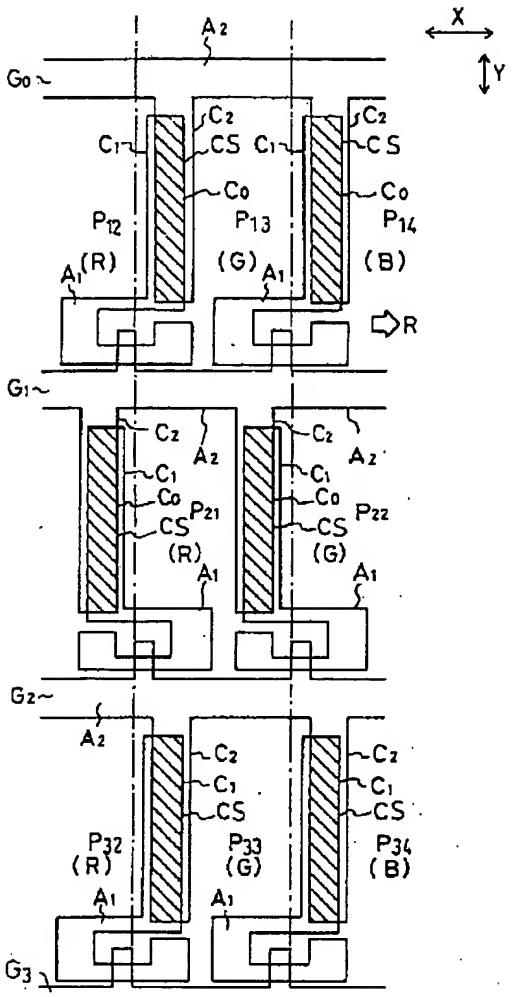
[Drawing 14]


S1
S2
S3
X
Y
G0
P11
(R)
P12
(G)
P13
(B)
II
II'
G1
CS
C1
C2
P21
III
(R)
P22
III'
(G)
P23
11
I'
12
112
I
G2
111
113
P31
(R)
P32
(G)
P33
(B)
G3

[Drawing 15]


P21
I
118
113
119
115
S1
C2
115
I'
(A)
110
111
11
112
114
C3
CS
110
C1
10
P11
S1
12
P12
S2
II
II'
(B)
C3
C2
C1
CS
10
C2
C1
C3
CS
P21
12
S2
P22
12
(C)
III
III'
C2
C1
C3
CS

[Drawing 16]



[Translation done.]